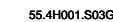


Project code: 91.4H001.001
PCB P/N : 55.4H001.XXX
REVISION : 06237-2(GCE, Hannstar)



ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCI Routing

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	USB4
4	MINIC1
5	BT
6	CCD
7	Finger
8	NEW
9	NC

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K (?)
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K (?)
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

2007/02/16
1. Page 33: Add SIO 87381 for FIR Issue.
2. Page 31, change KBC from 8768L to 8763L.
3. Page 33, del U33(LPC golden Finger).
4. Page 24/32, change ERC1/ERC2 due to 77.61021.02L is Obsoleted Part !
5. Page 37, del TC22/TC19.
6. Page 38, del TC1/TC4.
=====

2007/02/09
1. Page 14:Modify "Q14" "BTBTN1" "WLBTN1" symbol.
2. Page 36, 37, 38: Replace 0ohm with 0ohm pad.
=====

2007/02/08a
1. Page 14:Modify R428 to "FRONT_PWRLED#_1" and RN58 pin7 to "STBY_LED#_2" due to LED brightness issue.
2. Page 38:Replace "TC26" with "77.C1561.01L".
=====

2007/02/08
1. Page 10:Replace "R244" with "0603-PAD".
2. Page 36:Replace open power gap with close power gap.
3. Page 38:Add capacitor "TC26" for acoustic noise
=====

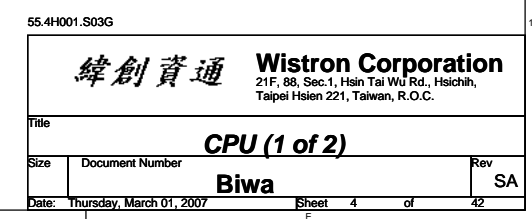
Crestline Strapping Signals and Configuration

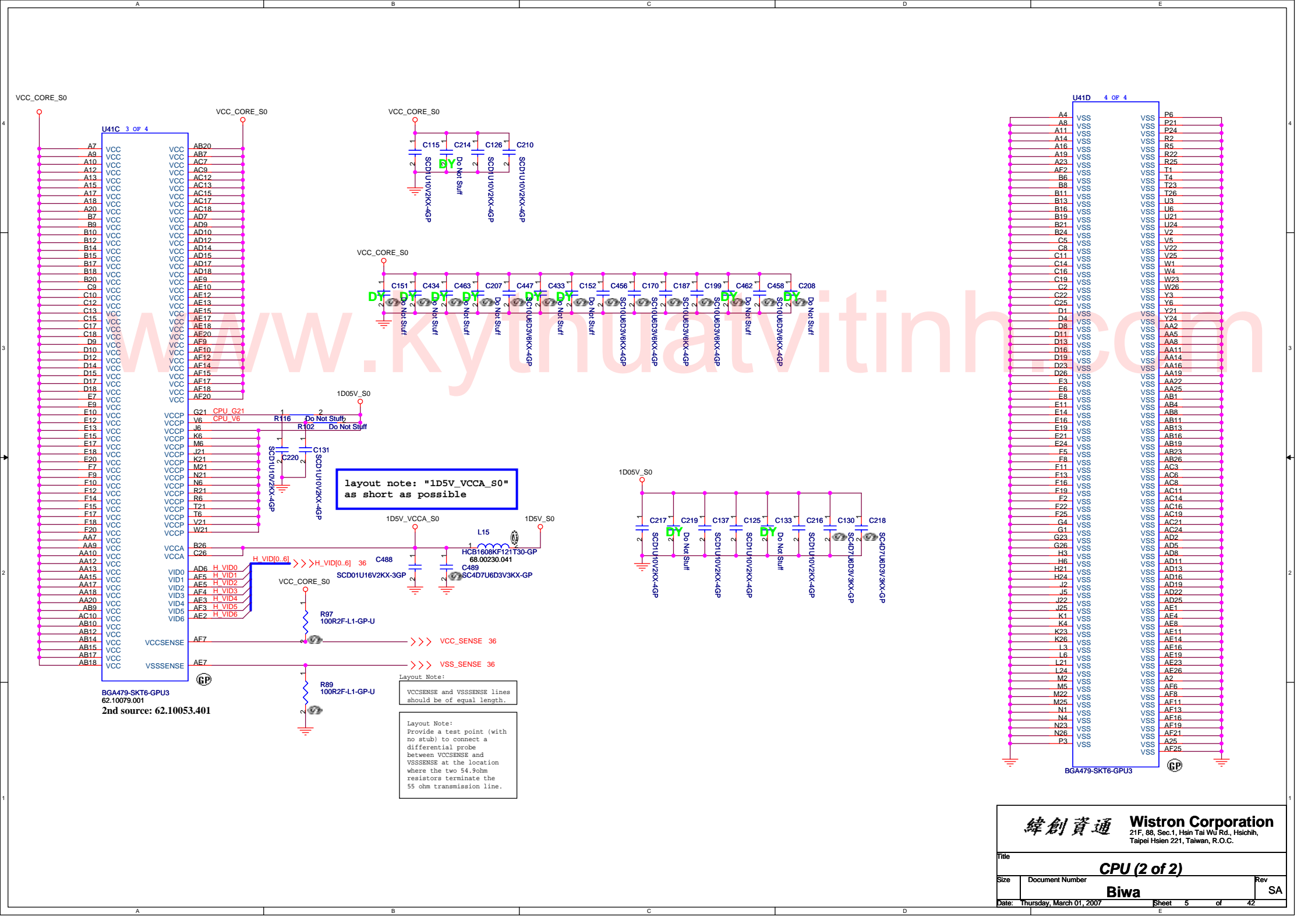
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

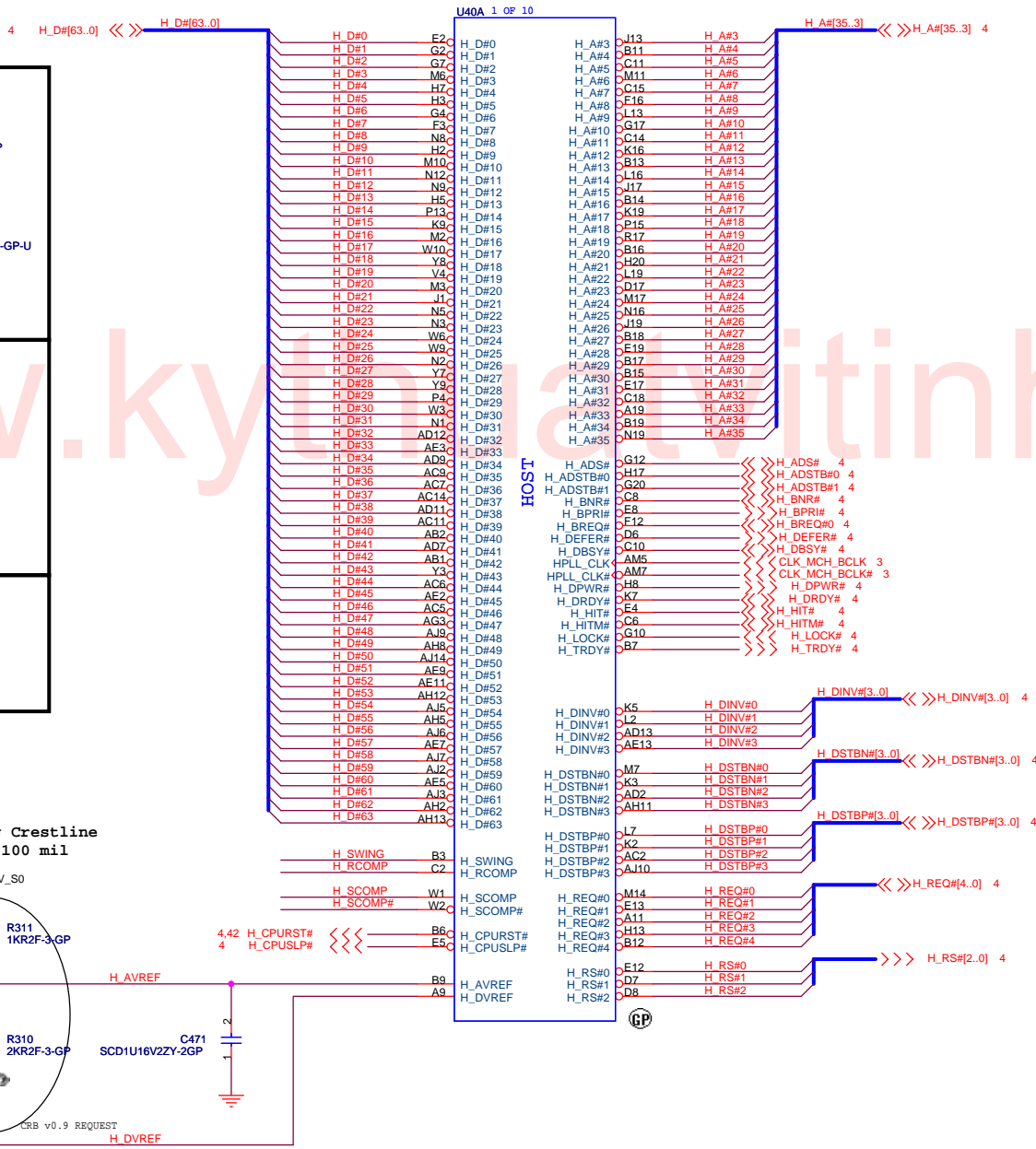
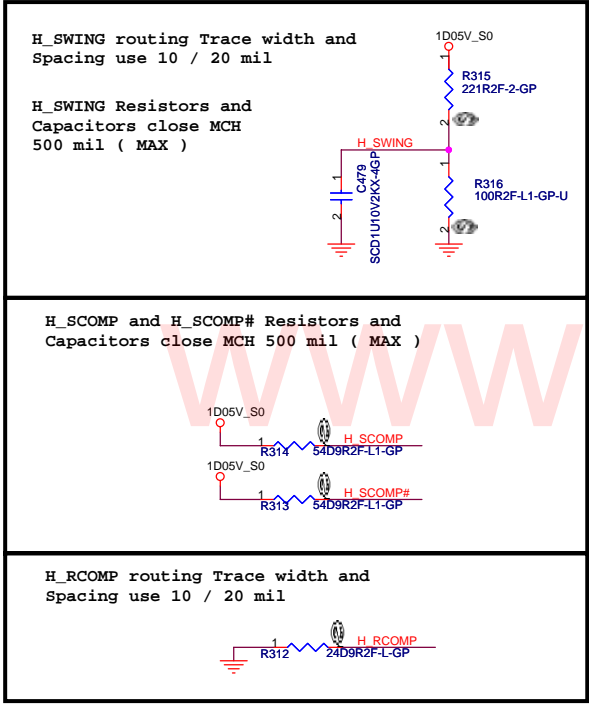
NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

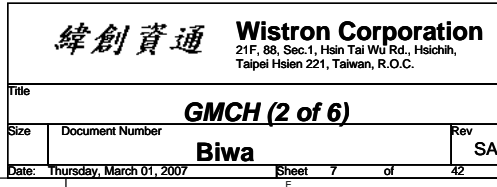
55.4H001.S03G

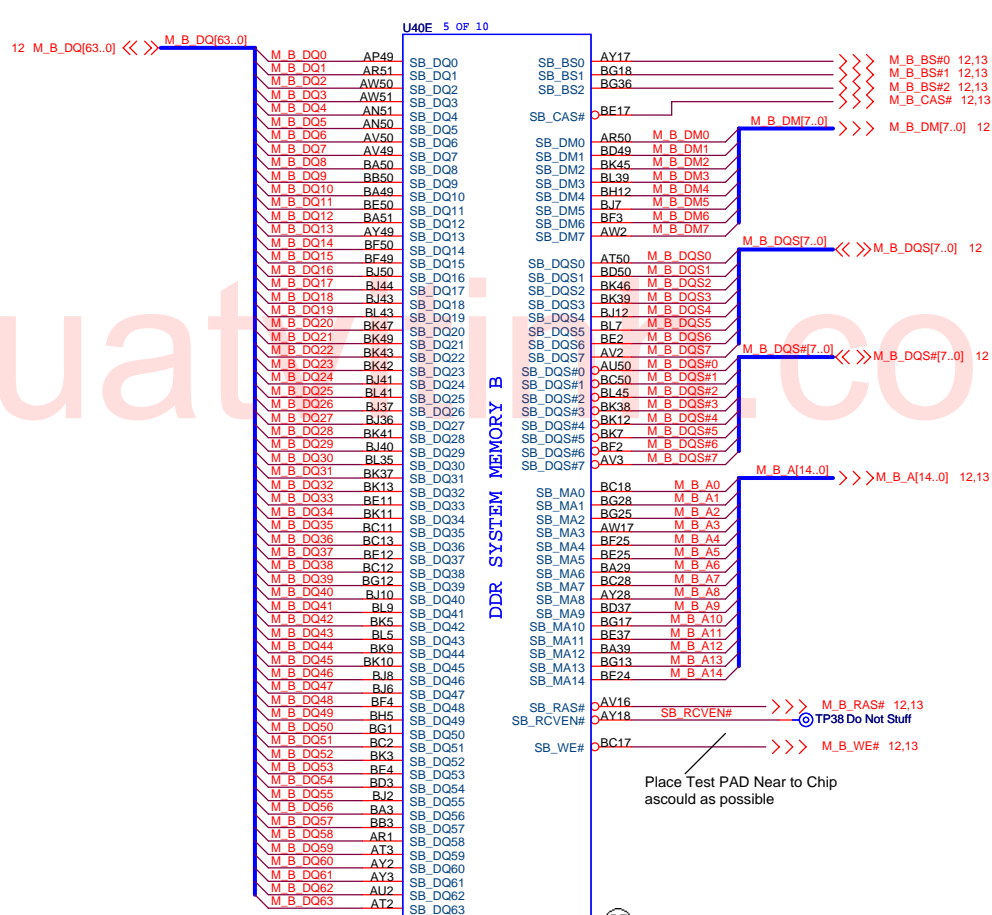
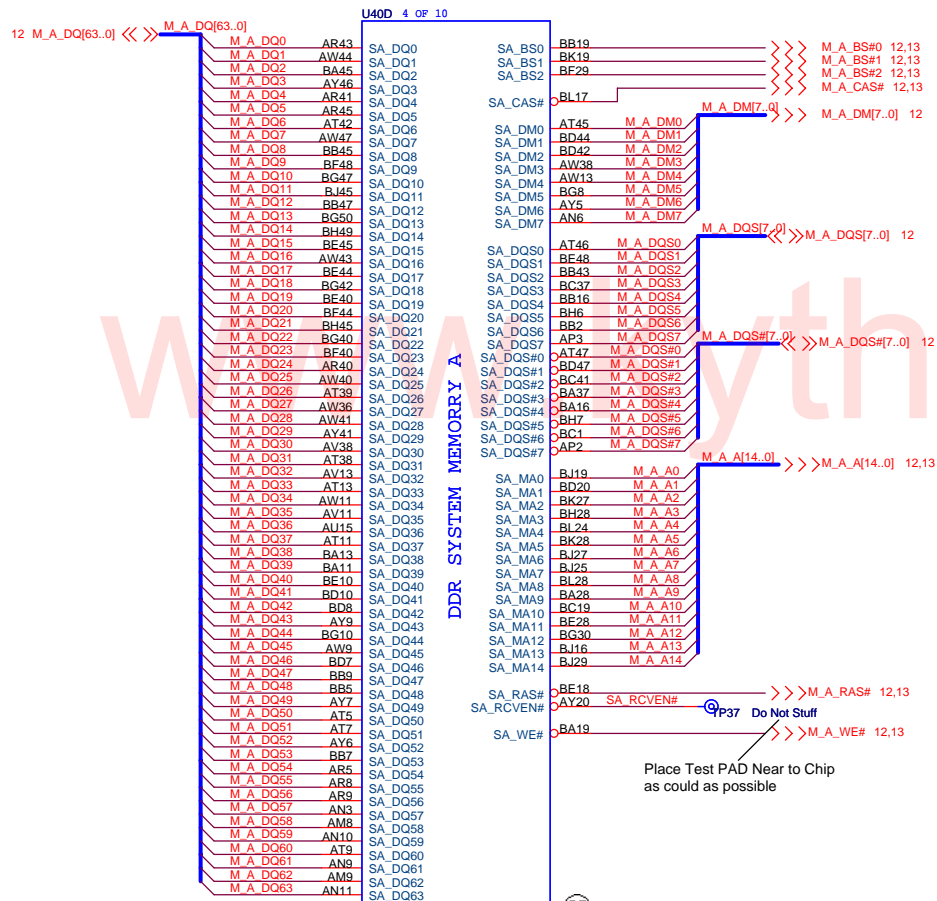
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reference			
Size A3	Document Number	Rev	-2
Date: Thursday, March 01, 2007		Sheet 2	of 42

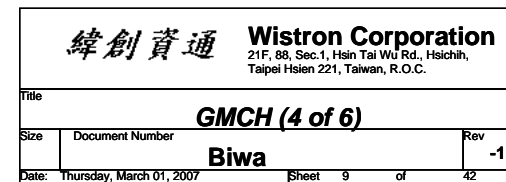
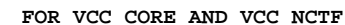


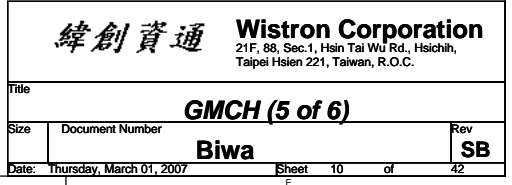


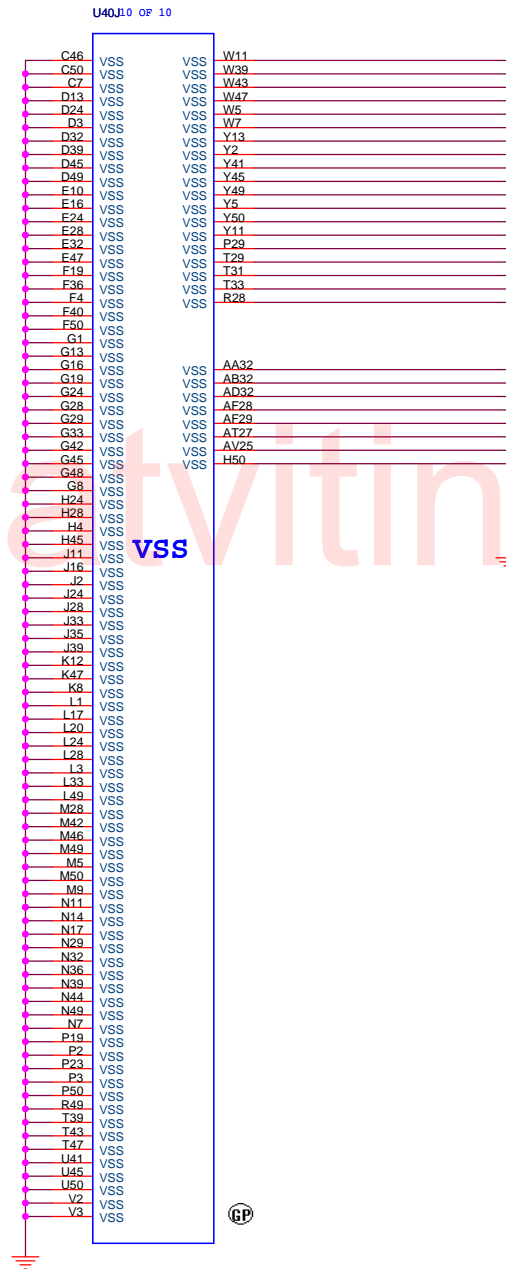
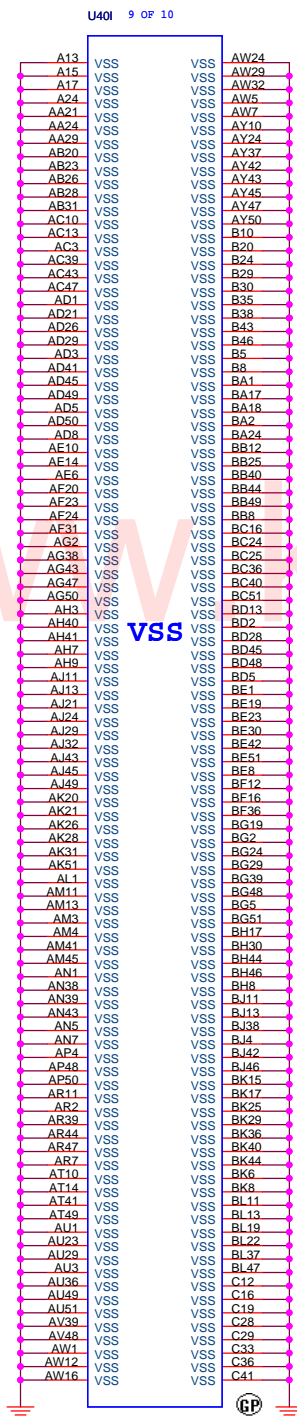


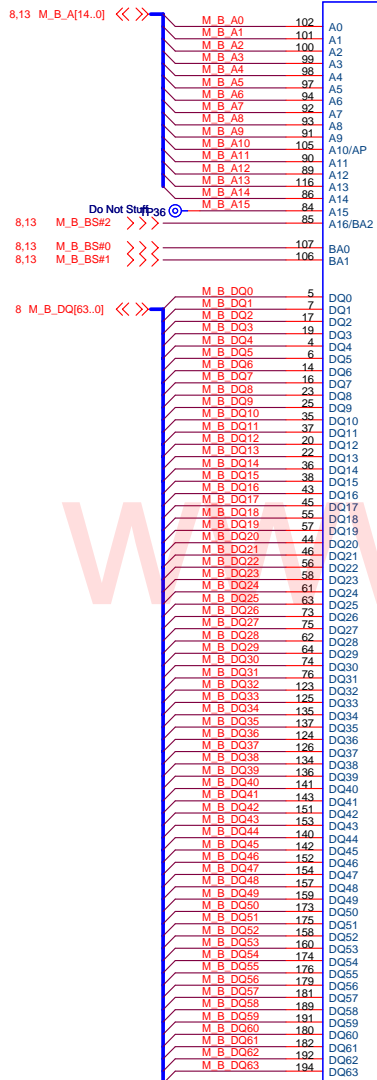










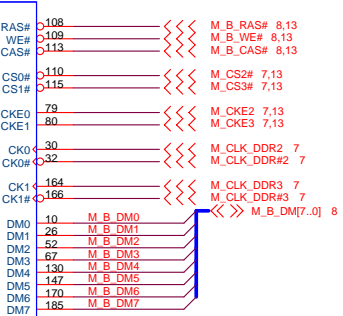


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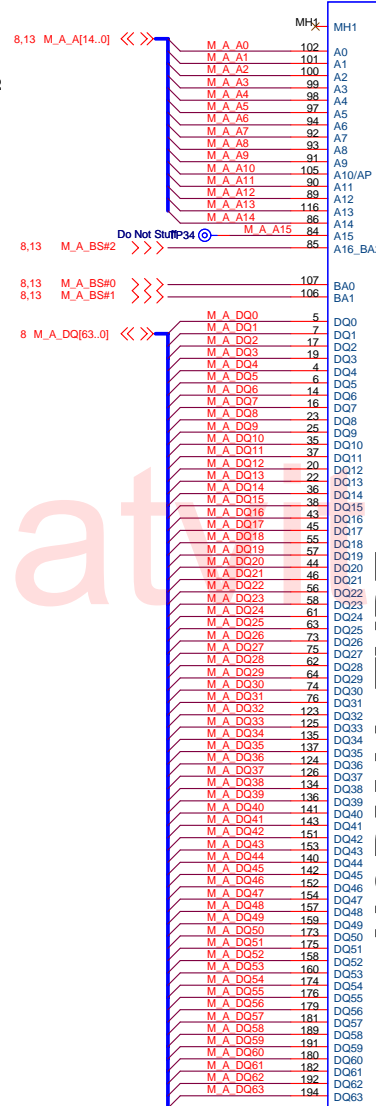
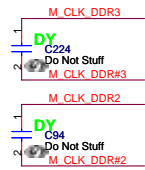
62.10017.A61

2nd source: 62.10017.A51

High 9.2mm



Place near DM2

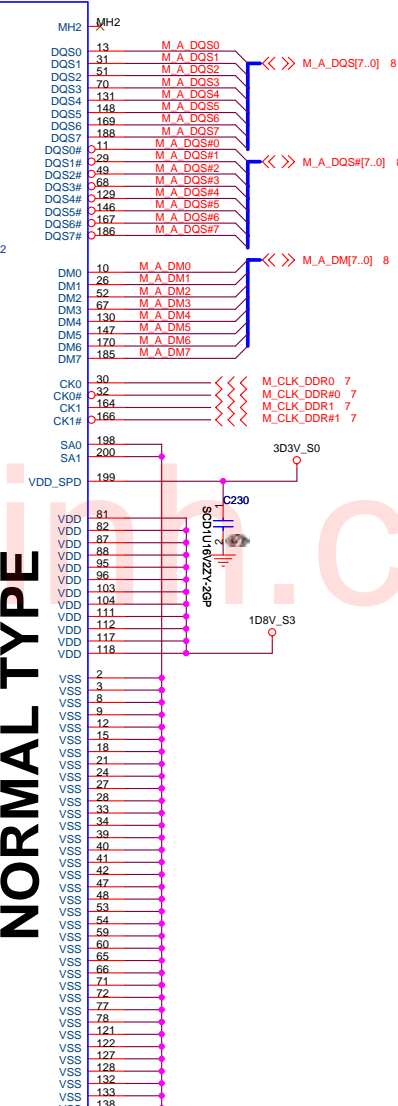


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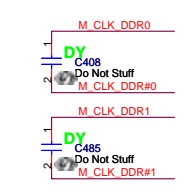
62.10017.661

High 5.2mm

2nd source: 62.10017.A41



Place near DM1



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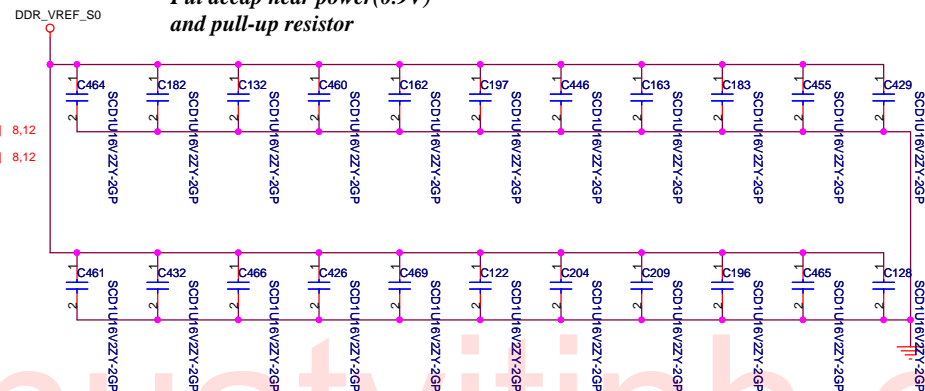
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Title				
DDR2 Socket				
Size	Document Number			Rev
	Biwa			SA
Date:	Thursday, March 01, 2007	Sheet	12	of 42

DDR_VREF_S0 *Put decap near power(0.9V) and pull-up resistor*



*Put decap near power(0.9V)
and pull-up resistor*



Place these Caps near DM1

1.8V_S3

C120

SC2322,6B3V3Mx+GP

C200

SC2322,6B3V3Mx+GP

C160

SC2322,6B3V3Mx+GP

C190

SC2322,6B3V3Mx+GP

C144

SC2322,6B3V3Mx+GP

C173

SCD1U6V2ZT-2G-F

C113

SCD1U6V2ZT-2G-F

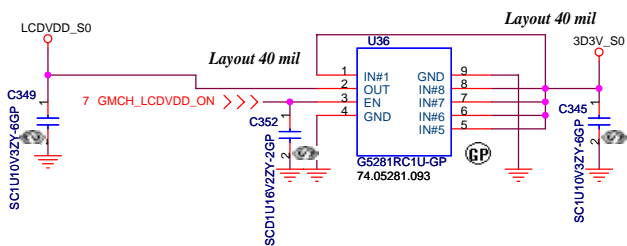
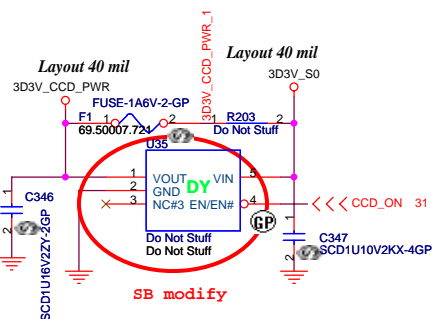
C186

SCD1U6V2ZT-2G-F

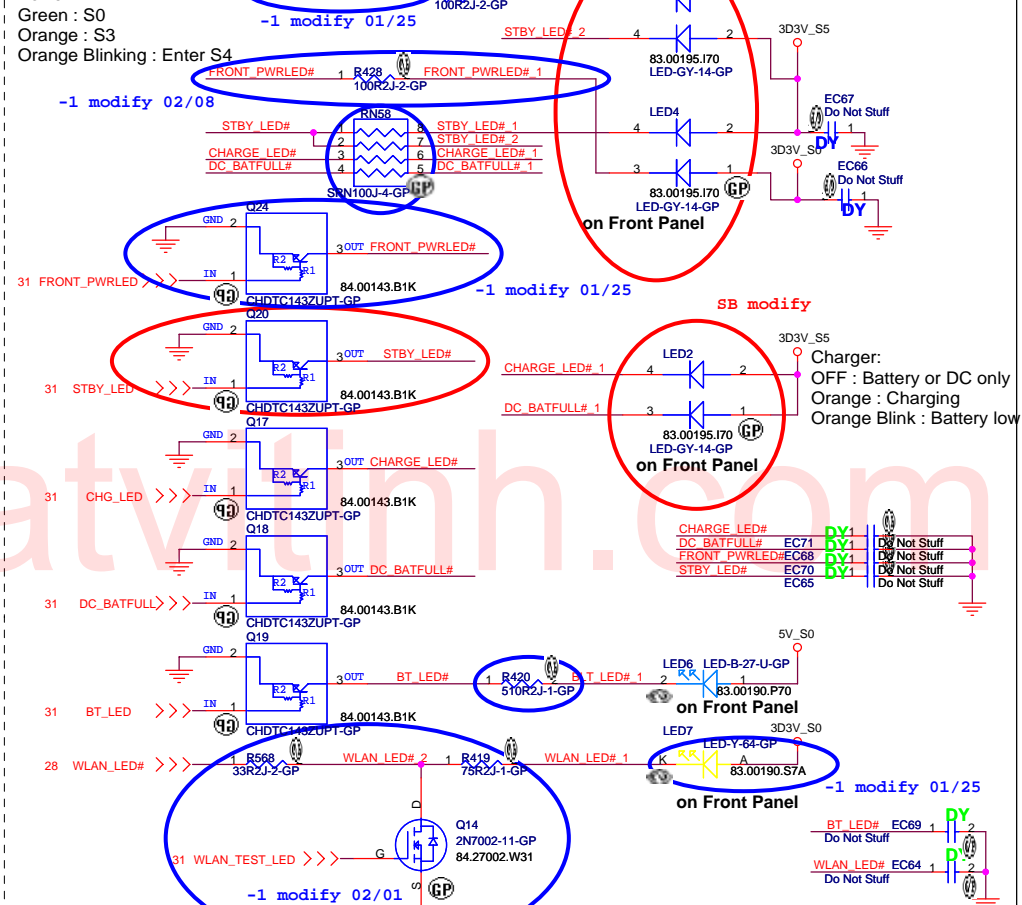
C171

SCD1U6V2ZT-2G-F

Ground



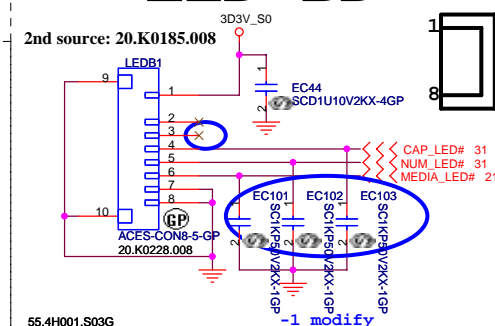
```
Green : S0
Orange : S3
Orange Blinking : Enter S4
```

[illegible]

2nd source: 62.40068.001

-1 modify 01/31 for EMI

LED BD

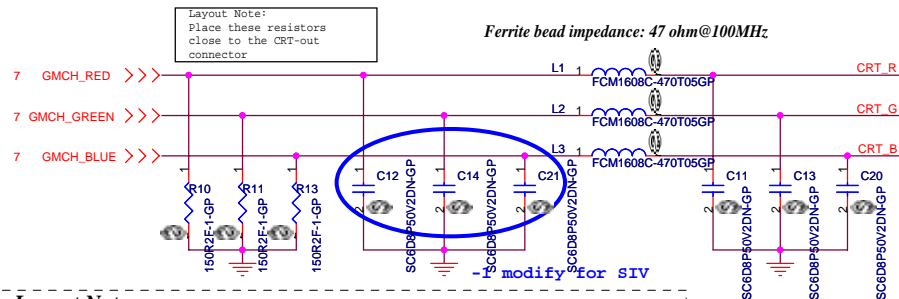


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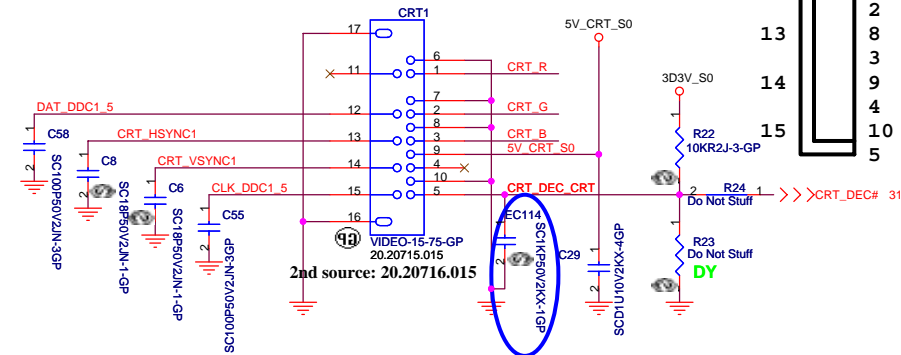
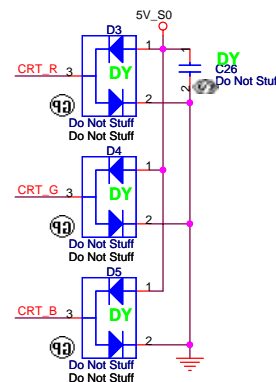
Title			
LCD CONN & LED			
Size	Document Number		Rev
	Biwa		-1
Date:	Thursday, March 01, 2007	Sheet 14 of	42

CRT I/F & CONNECTOR

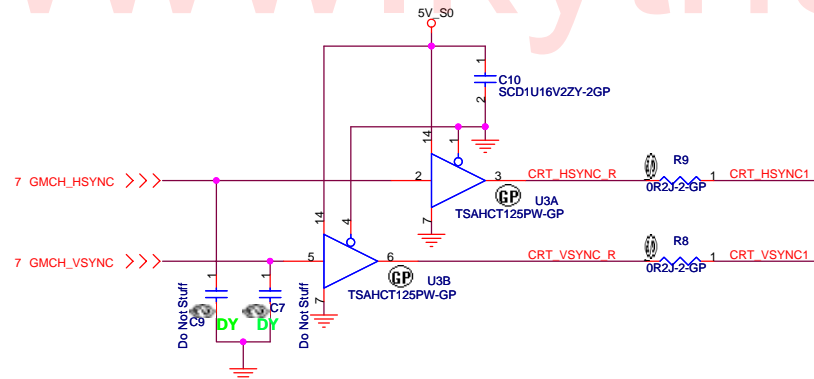
11	6
12	1
13	7
14	2
15	8
	3
	9
	4
	10
	5



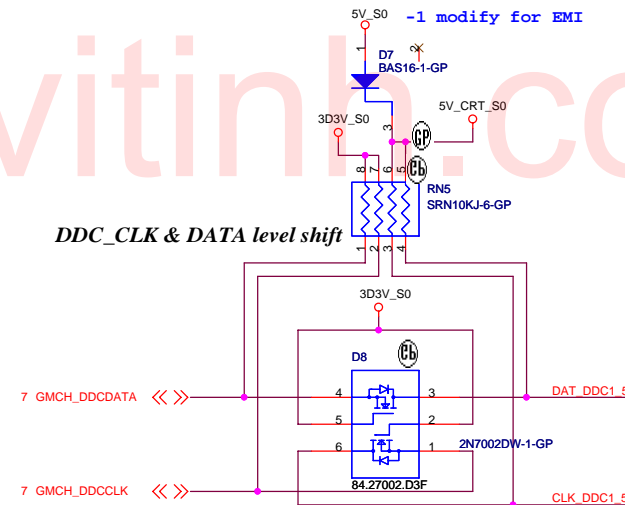
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



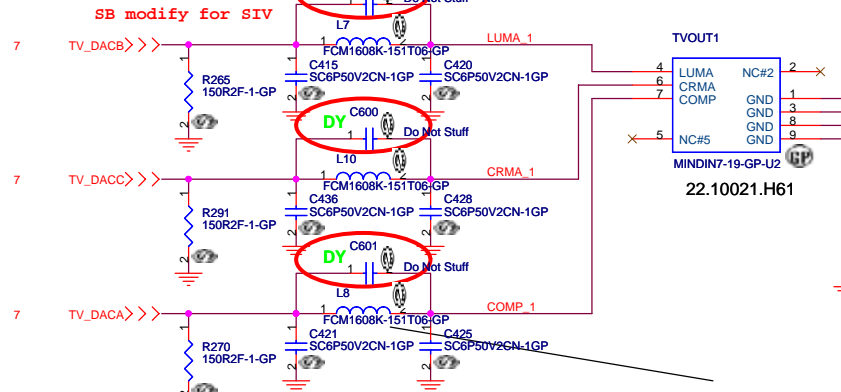
Hsync & Vsync level shift



DDC_CLK & DATA level shift

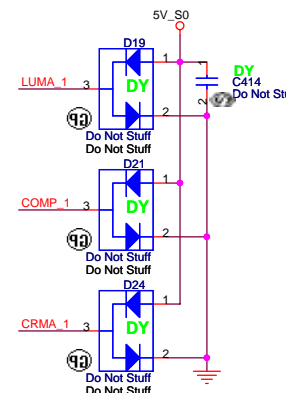


TV CONN



TVOUT1
LUMA 1
CRMA 1
COMP 1

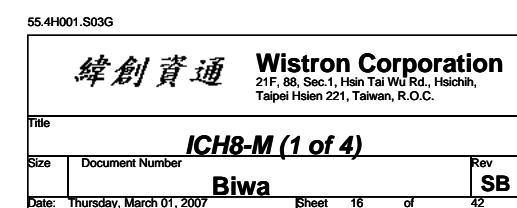
22.10021.H61

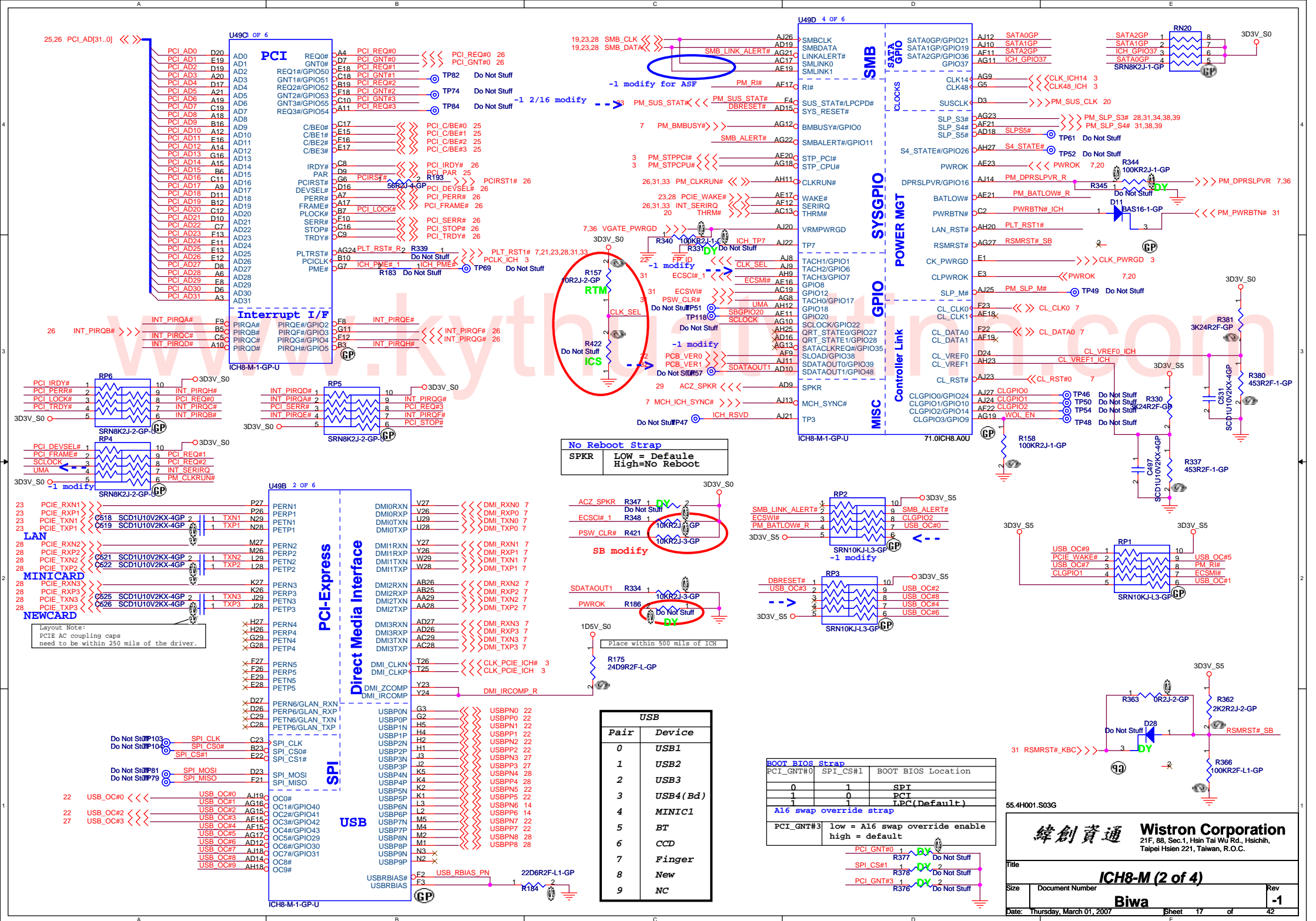


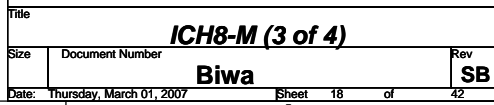
Ferrite bead impedance: 150 ohm@100MHz; 100mA(min) design recommend

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Title	CRT/TV Connector	Rev	-1
Size	Document Number		
Date:	Thursday, March 01, 2007	Sheet	15 of 42



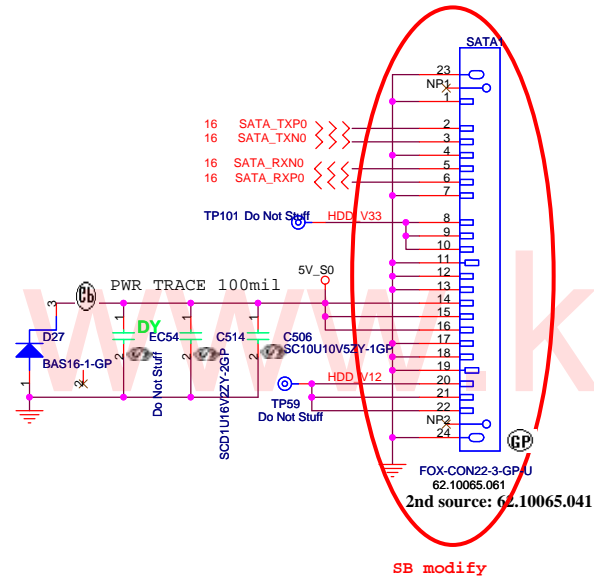




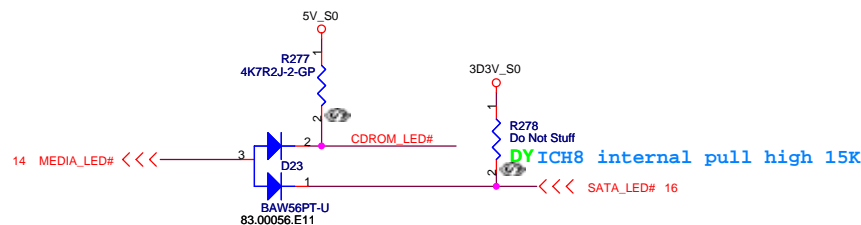
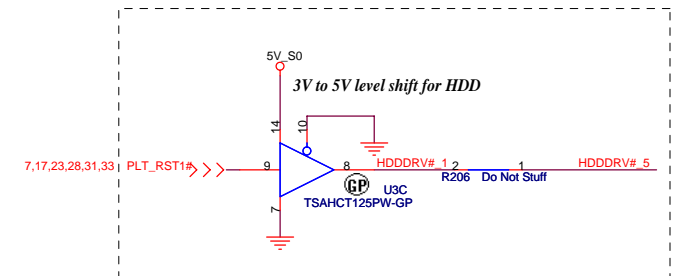
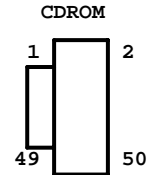
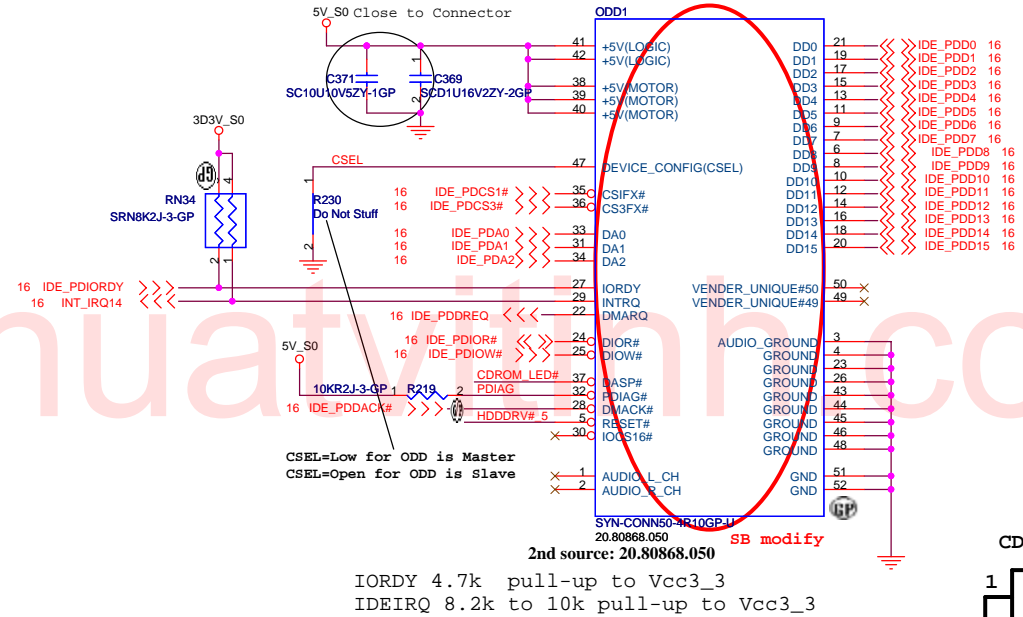


SMBUS

SATA Connector



ODD Connector

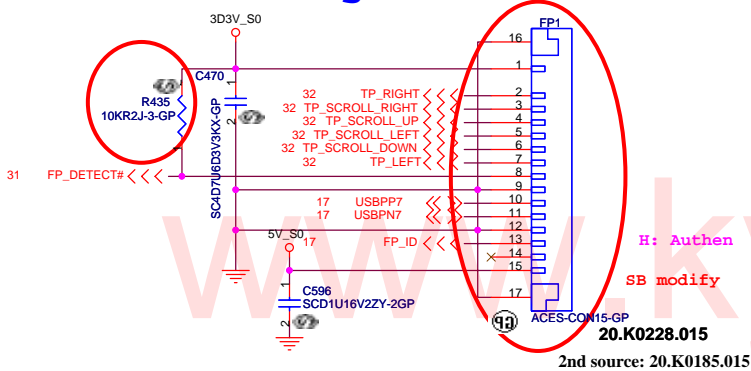


55.4H001.S03G

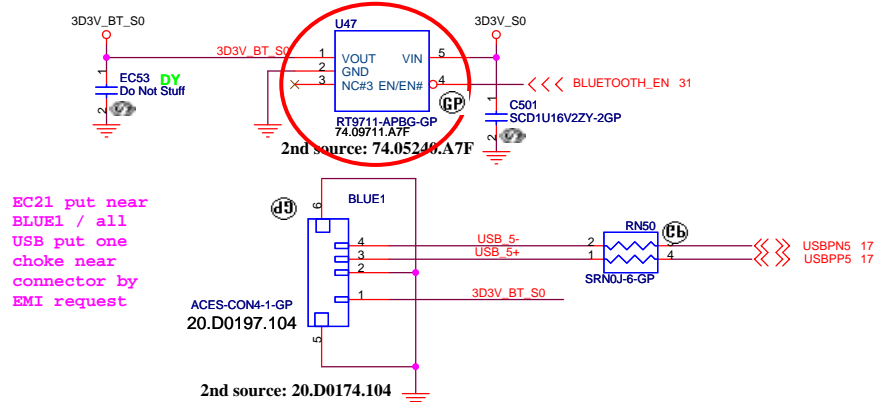
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Title
HDD and CDROM
Size Document Number
Biwa
Date: Thursday, March 01, 2007 Sheet 21 of 42
Rev
SB

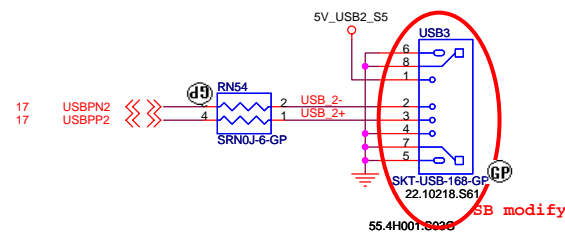
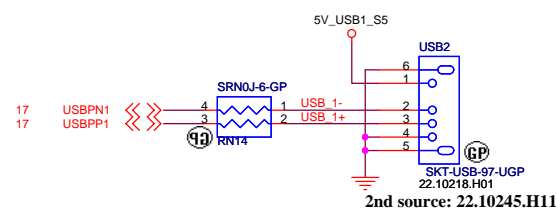
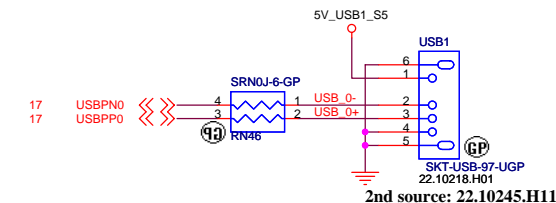
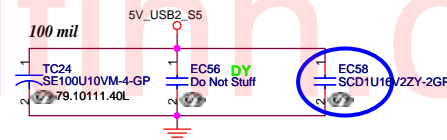
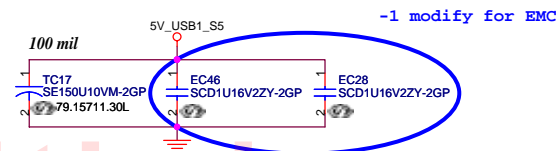
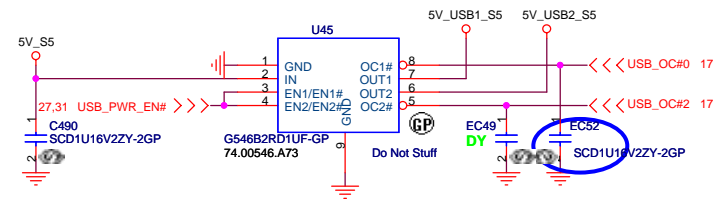
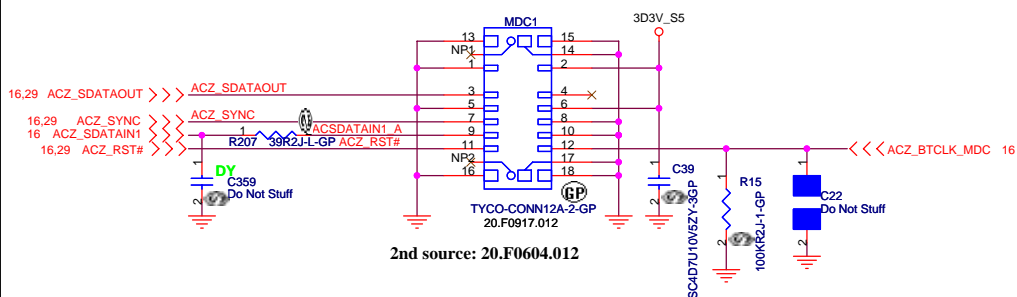
Finger Print



BLUETOOTH MODULE



MDC 1.5 CONN

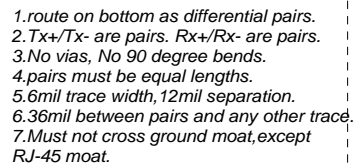


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Title			
USB / MDC / BLUETOOTH / FP			
Size	Document Number	Rev	
	Biwa	-1	
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LAN Connector

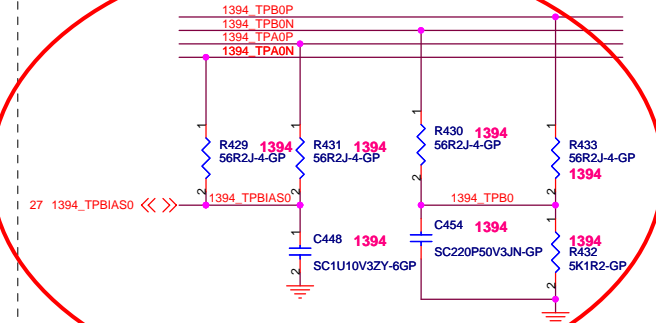
A2(+) A1(-)::GREEN
A2(+) A3(-)::ORANGE



DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

CLOSE TO CHIP



SB modify

TI PCI7412

IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQB#
INTC-->:INT_PIRQF#
INTD-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0

INTA# CARBUS 1 (INT_PIRQG#)
 INTB# 1394 (INT_PIRQB#)
 INTC# Flash Media (INT_PIRQF#)
 INTD# SD Host (INT_PIRQG#) share
 MFUNC4: use bit 19-16 Register define.

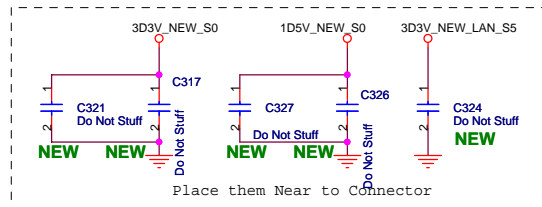
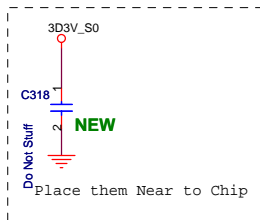
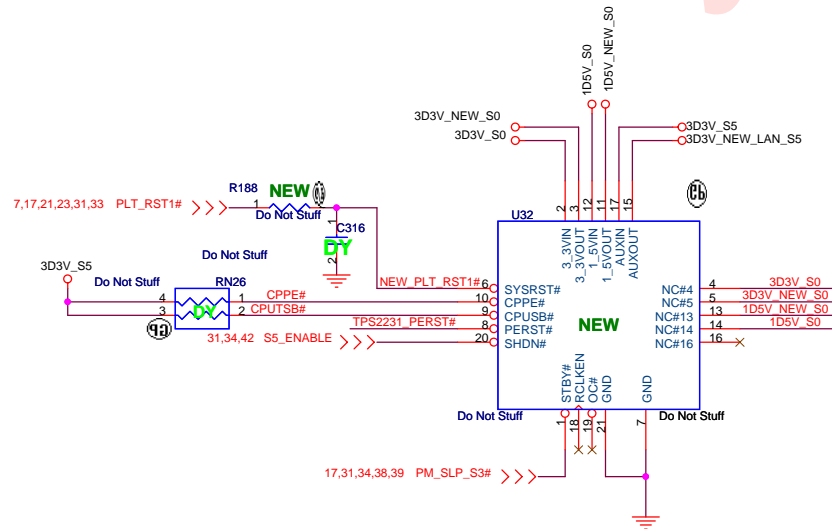
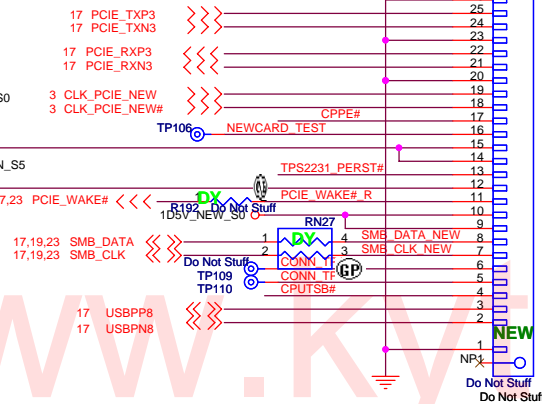
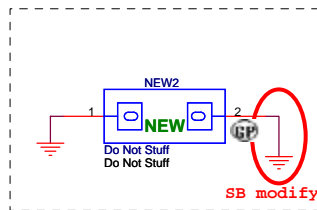
55.4H001.S03G

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 Taipei Hsien 221, Taiwan, R.O.C.

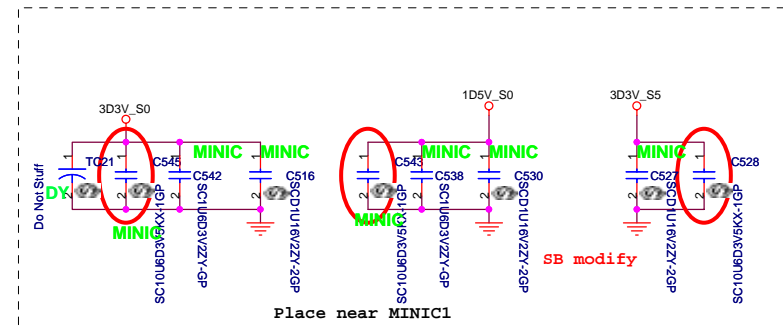
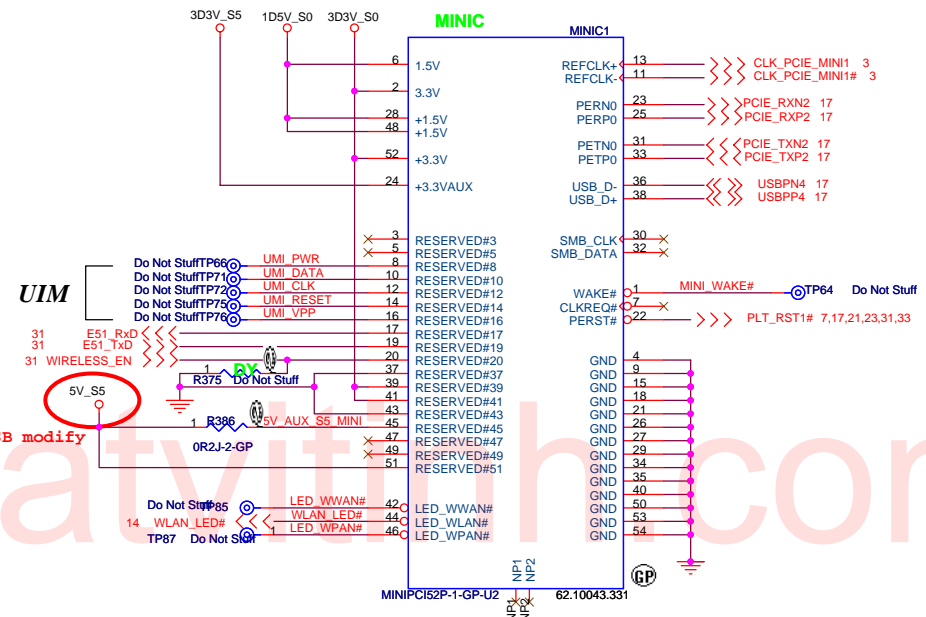
Title		TI PCI7412 (2 of 2)	
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		SB	

NEWCARD Connector

Reserve the symbol
for bottom side
connector

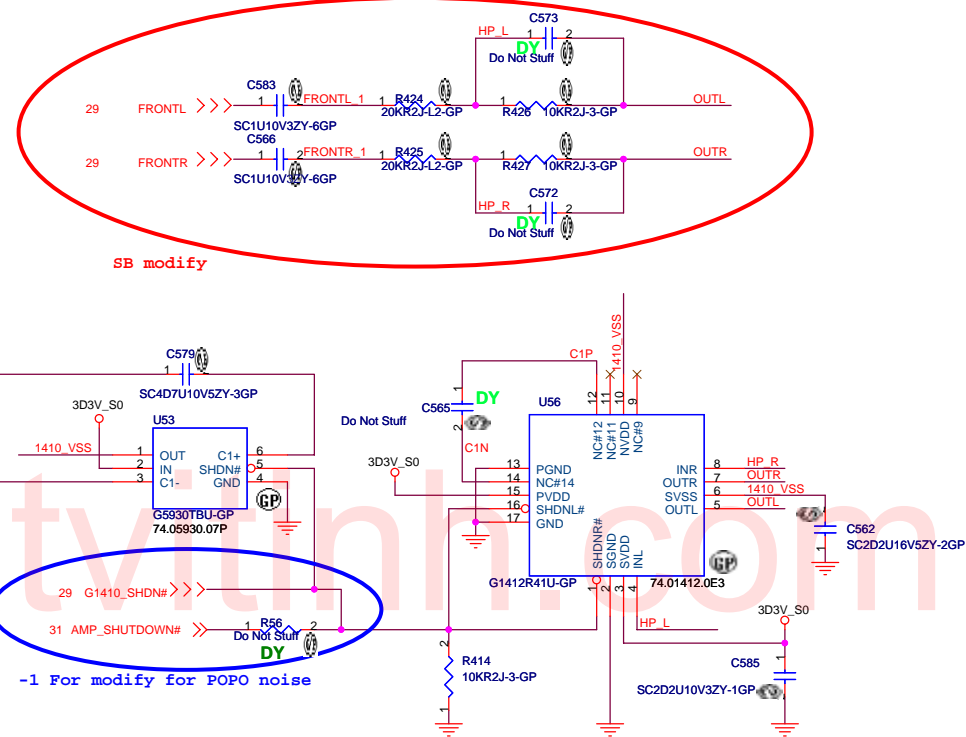
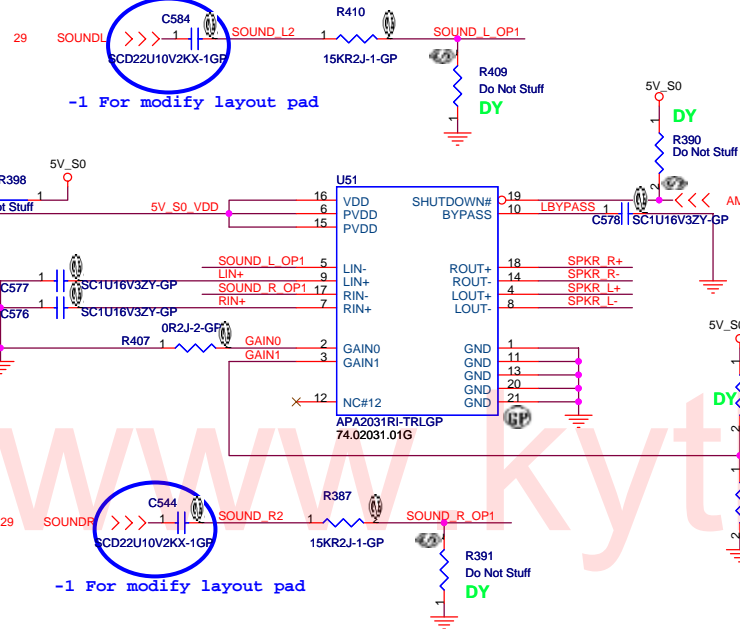


Mini Card Connector

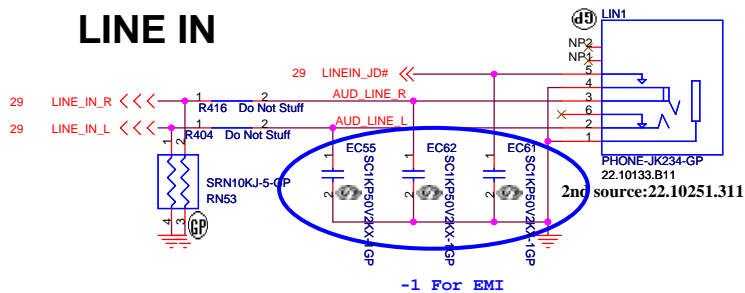


AUDIO OP AMPLIFIER

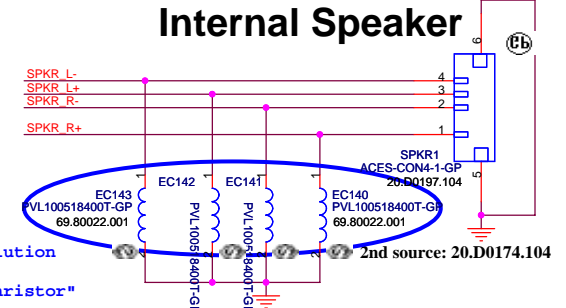
I/P signal level
need +5V level



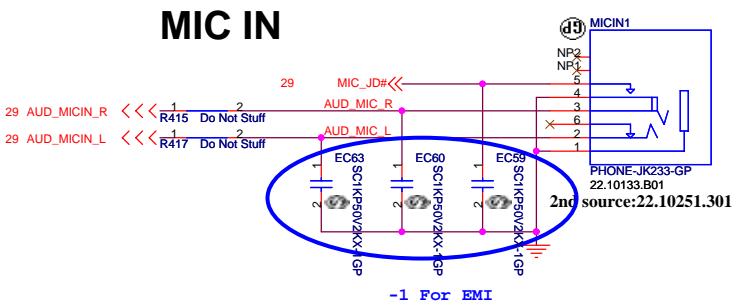
LINE IN



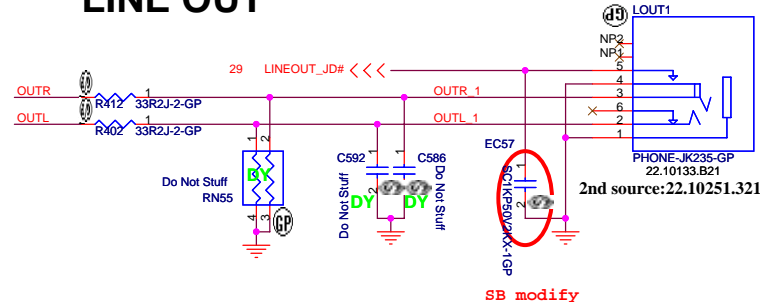
Internal Speaker



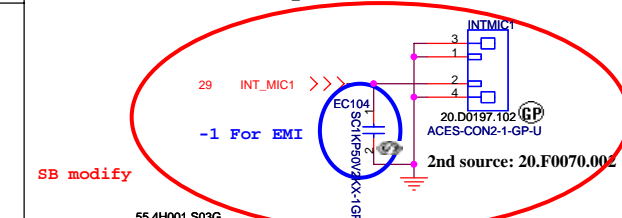
MIC IN



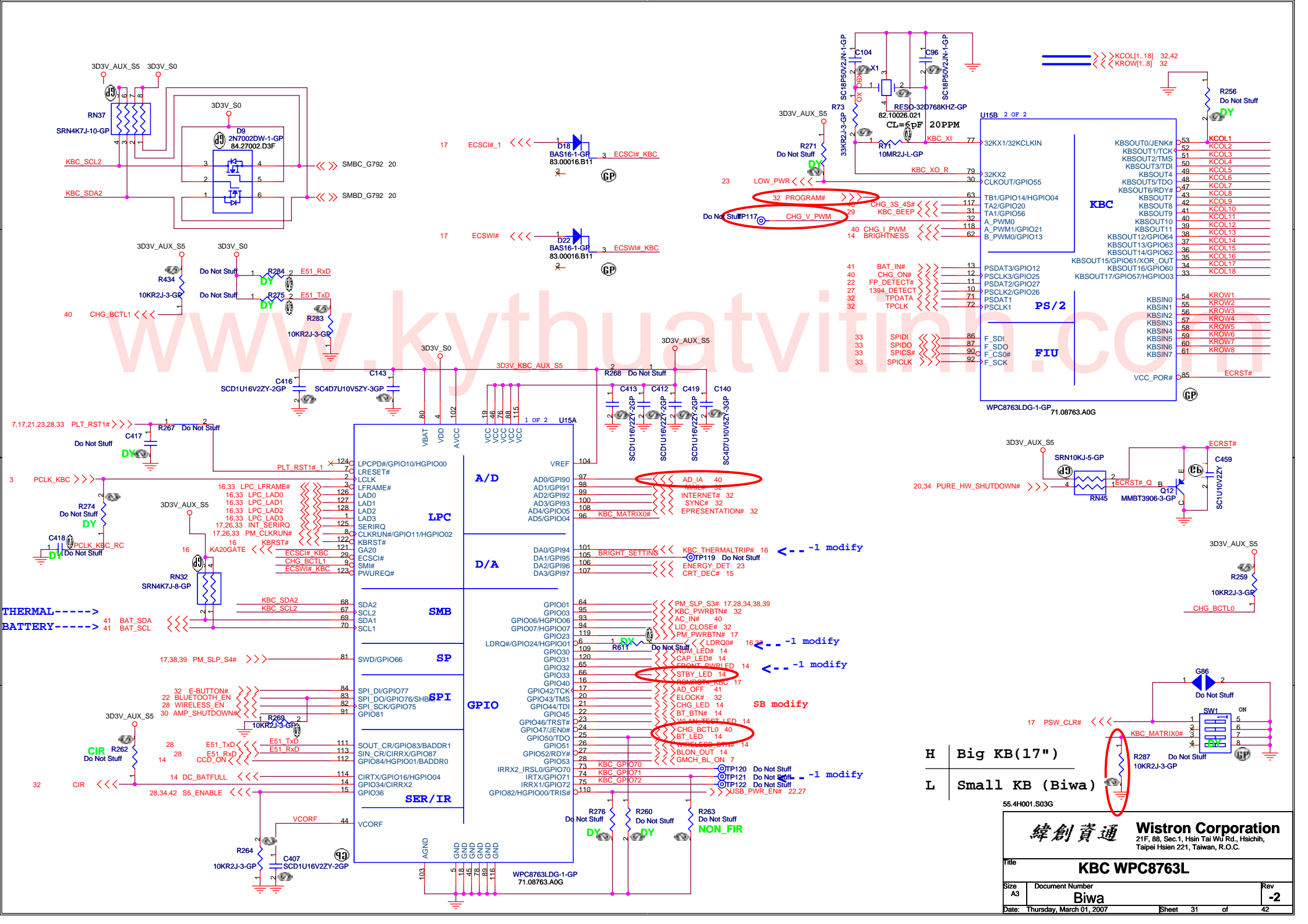
LINE OUT



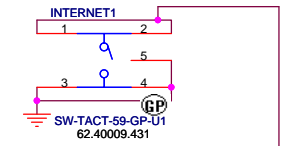
Internal Microphone



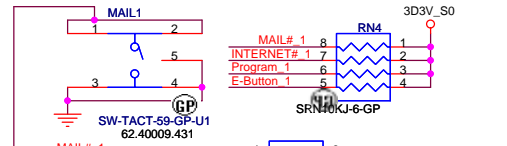
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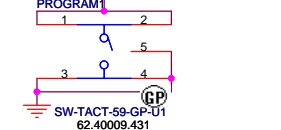
Internet Button



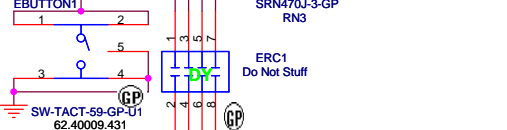
Mail Button



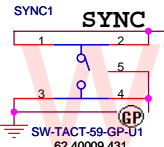
Program Button



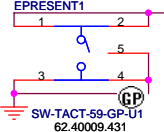
E-Button



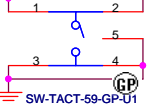
2nd source: 62.40009.561



EPRESENTATION

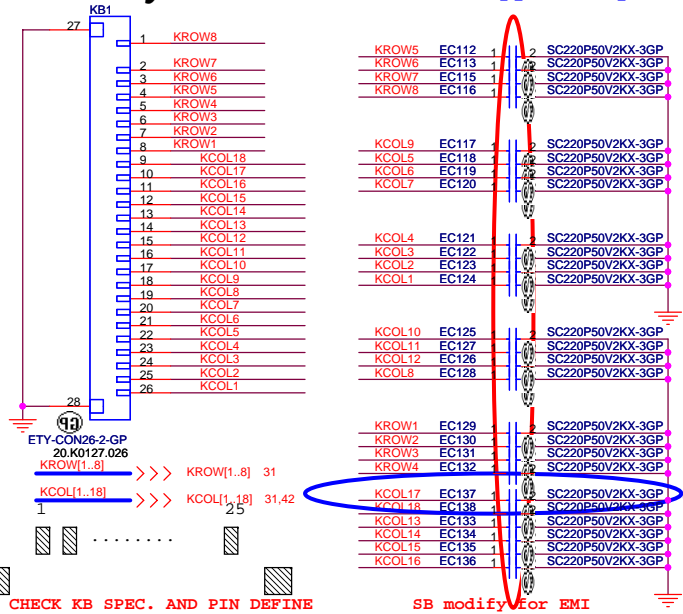


ELOCK



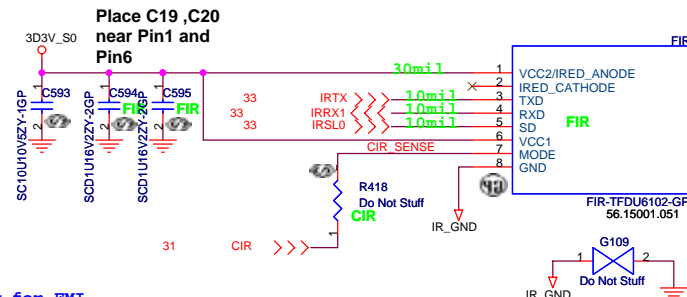
Internal KeyBoard CONN

EMI Bypass cap.



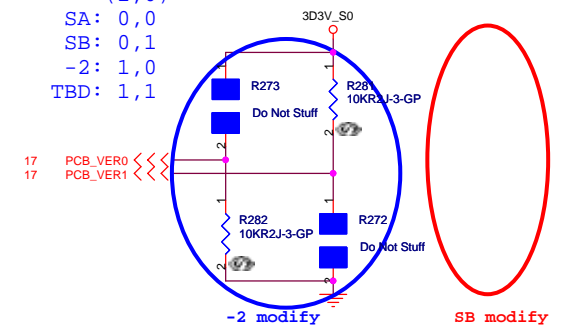
VISHAY FIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close
to U32



PlanarID

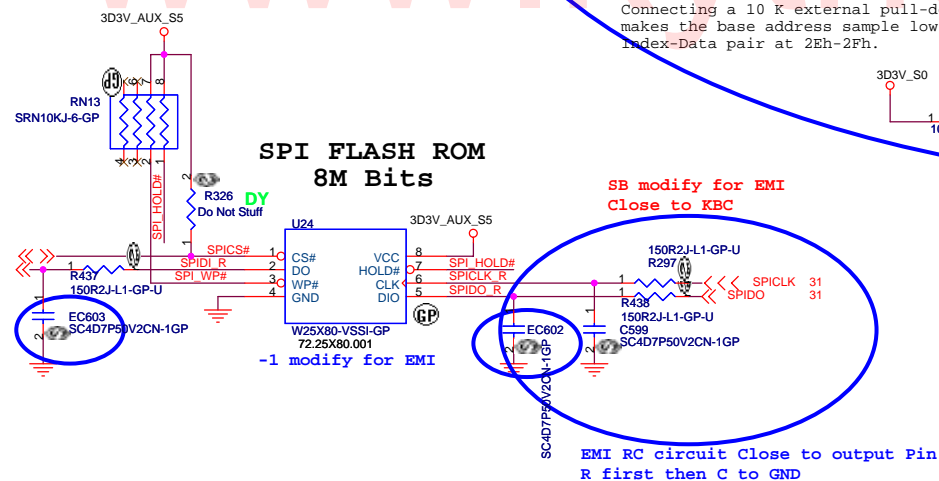
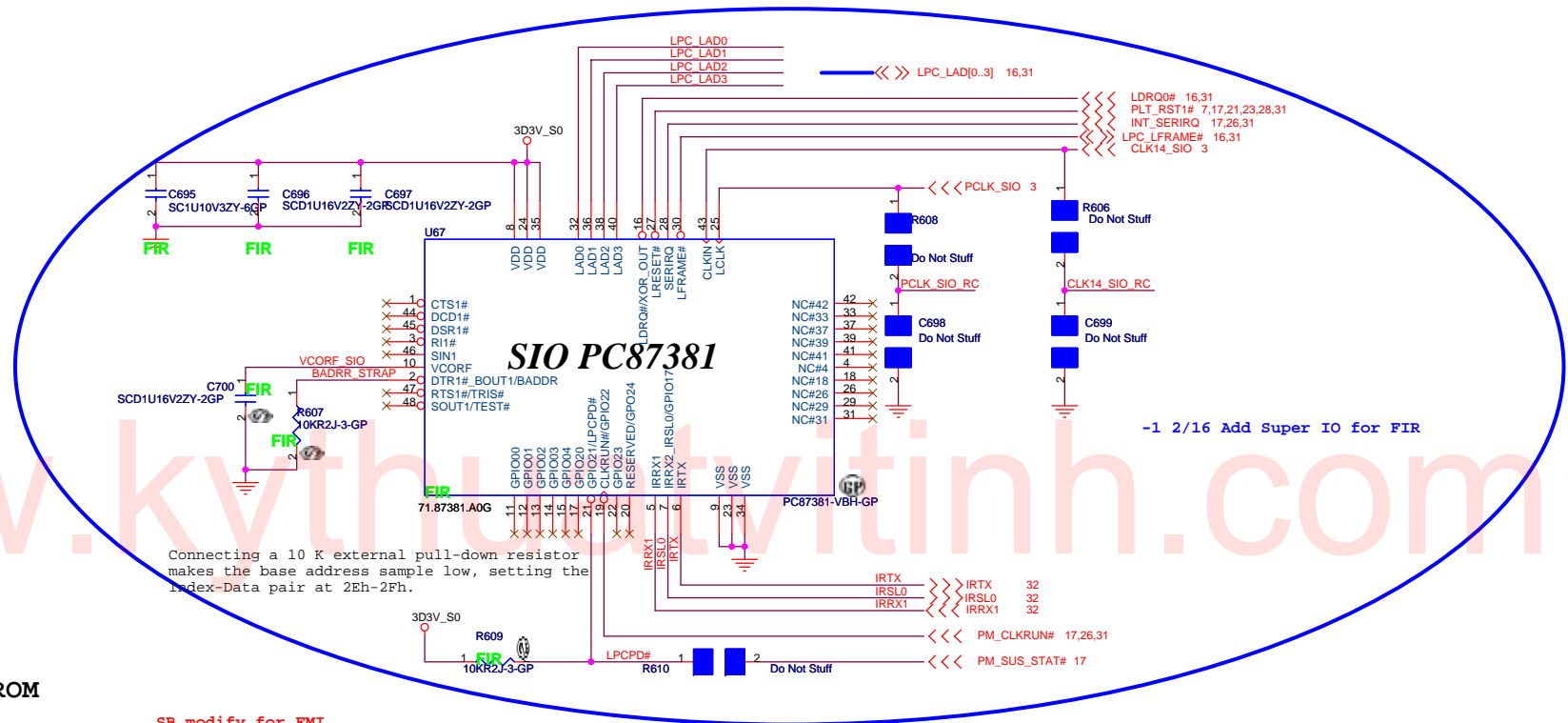
(1,0)
SA: 0,0
SB: 0,1
-2: 1,0
TBD: 1,1



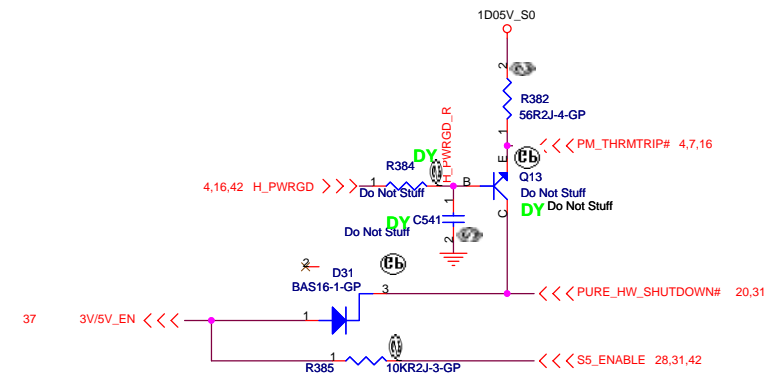
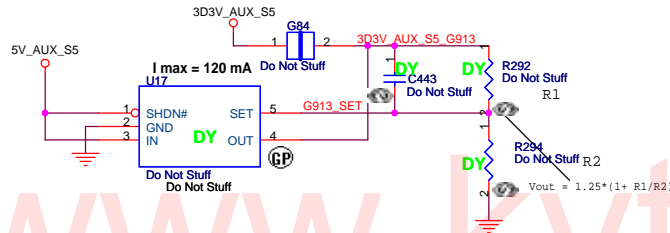
55.4H001.S03G

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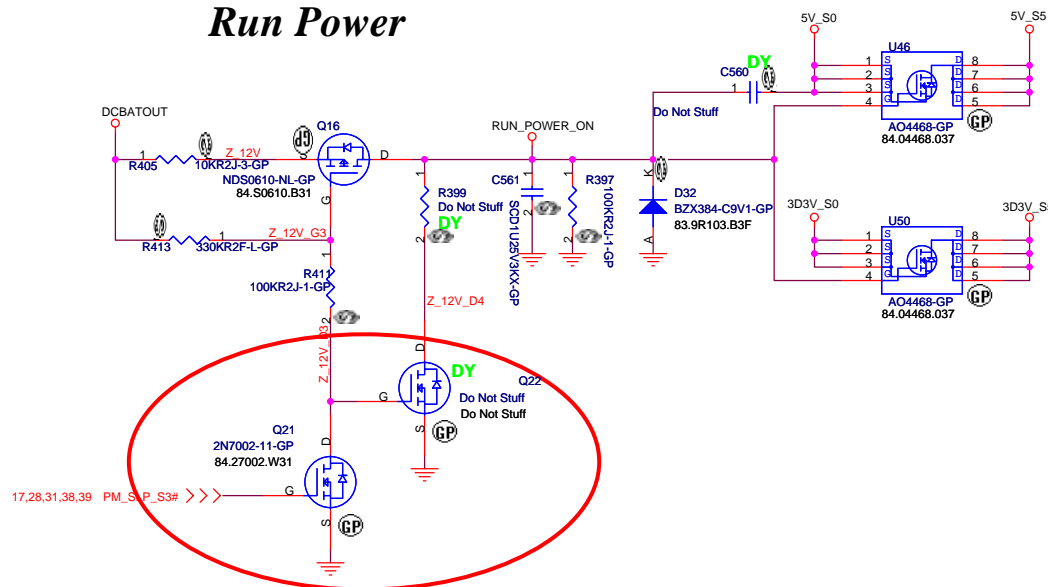
Title: BUTTONs / KB / TOUCHPAD / FIR
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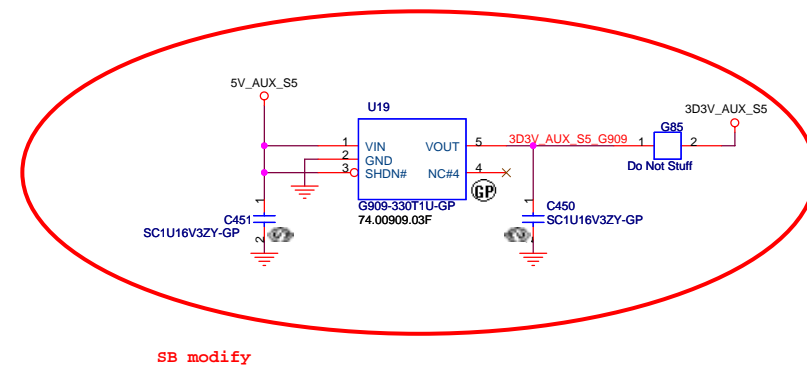
Aux Power 3D3V_AUX_S5



Run Power

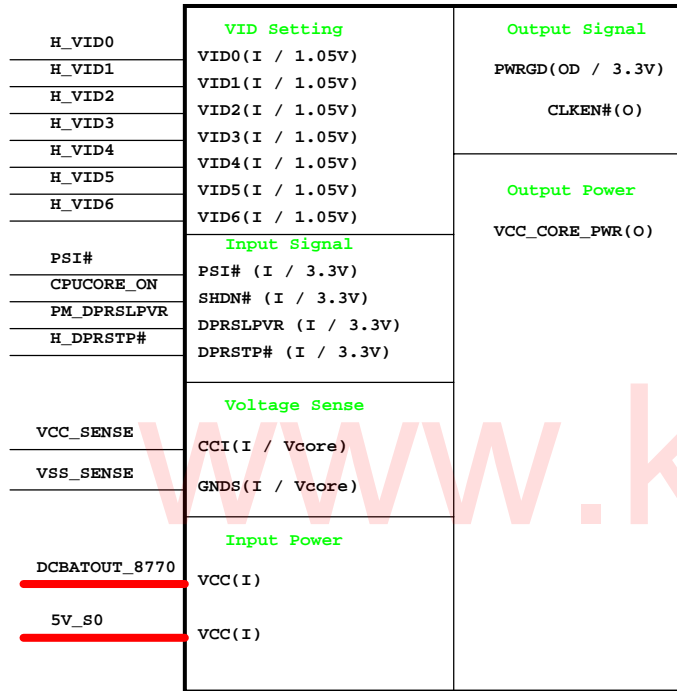


Aux Power 3D3V_AUX_S5

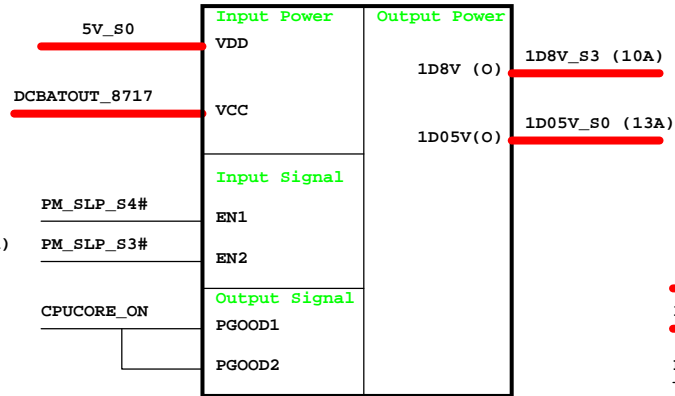


55.4H001.S03G

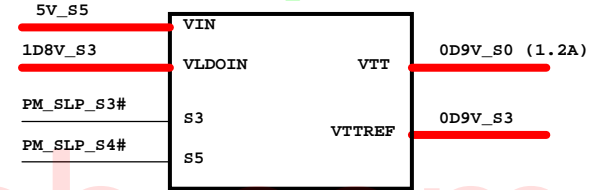
CPU_CORE
MAXIM MAX8770



MAX8717
1D8V/1D05V

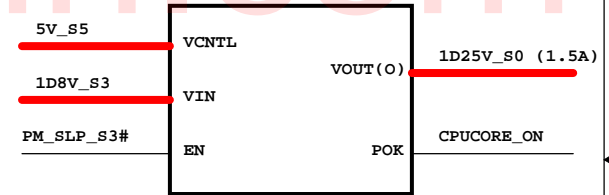


0D9V_S0



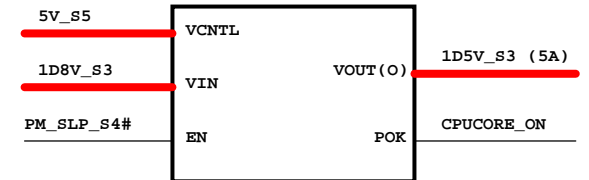
TPS51100

1D25V_S0



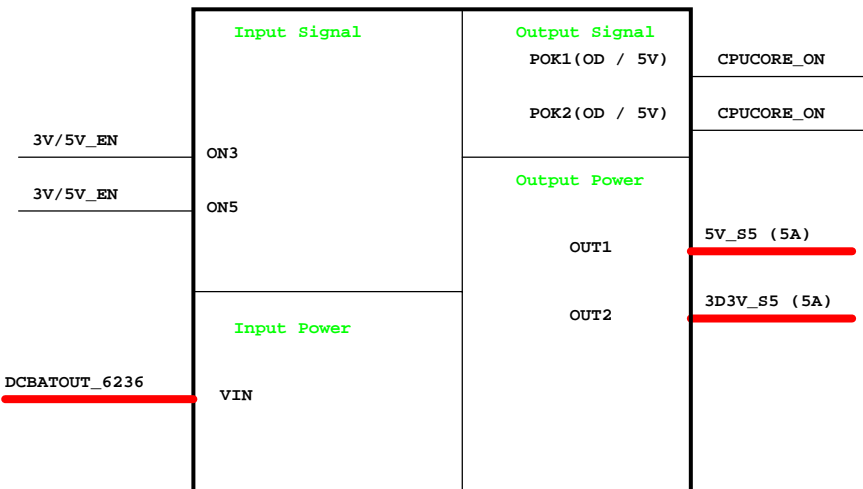
APL5915

1D5V_S3

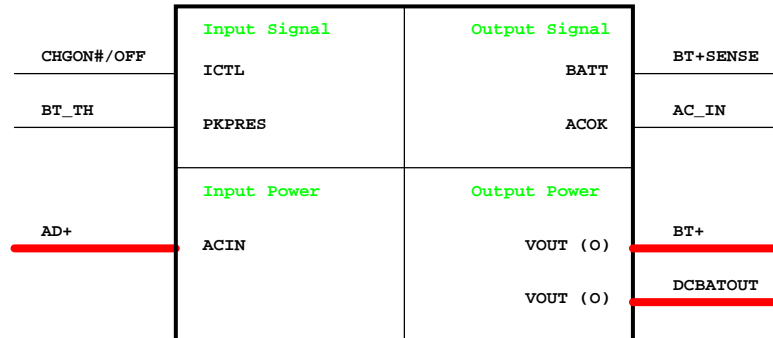


APL5912

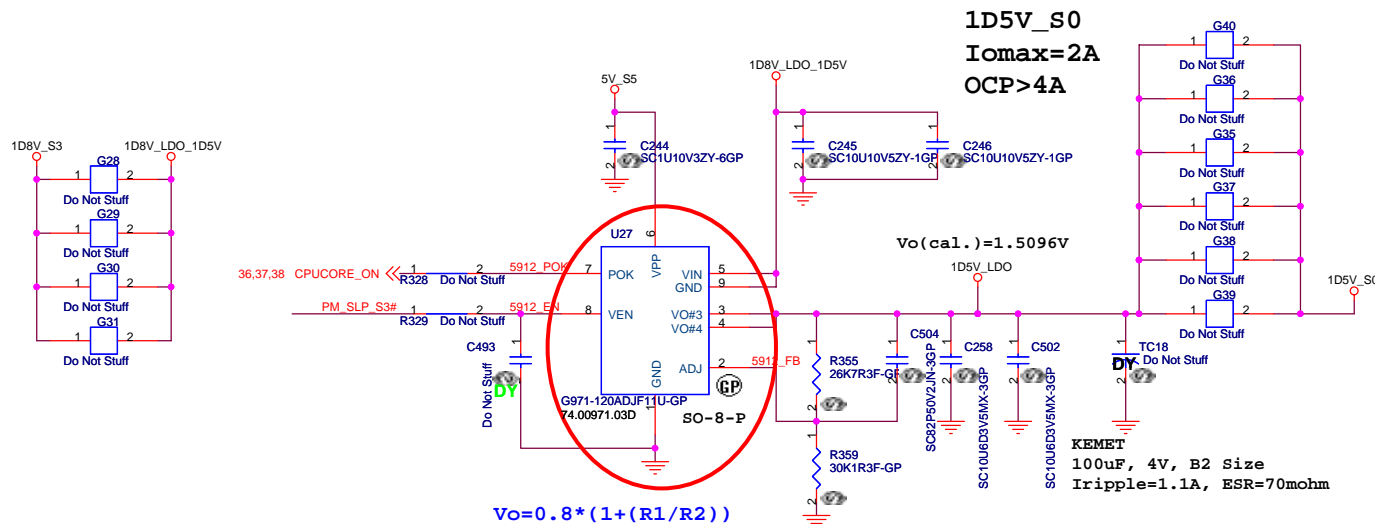
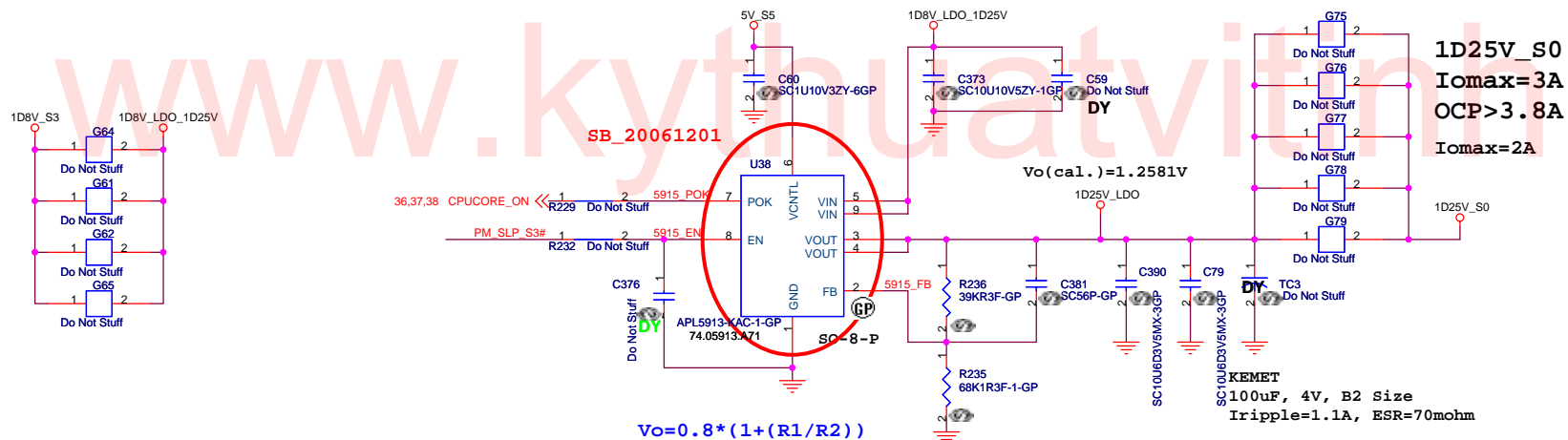
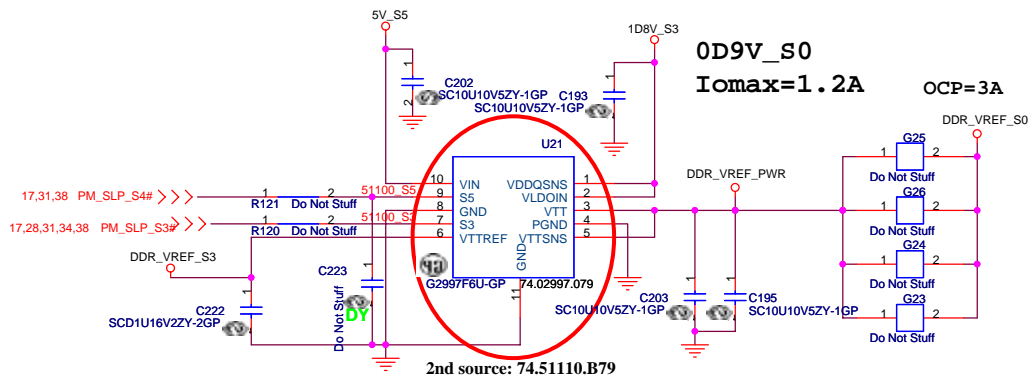
ISL6236
5V/3D3V



Charger ISL6255



55.4H001.S03G

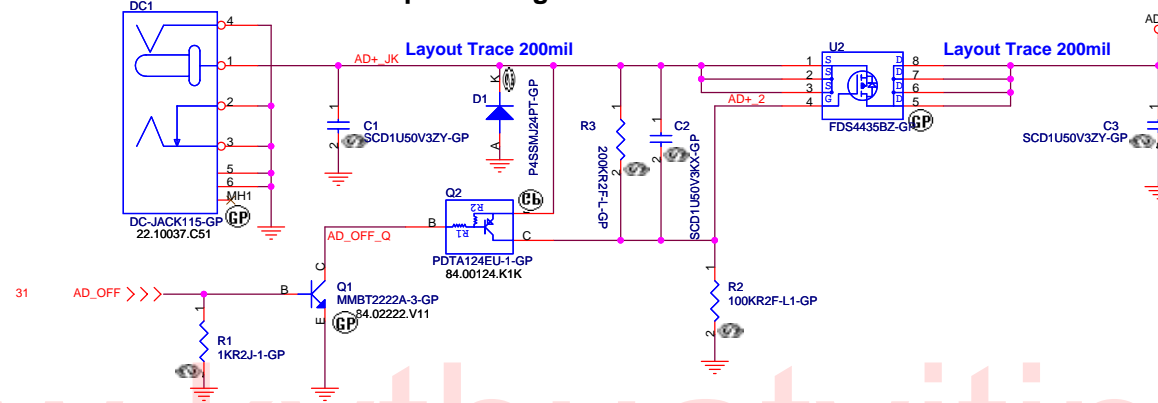


55.4H001.S03G

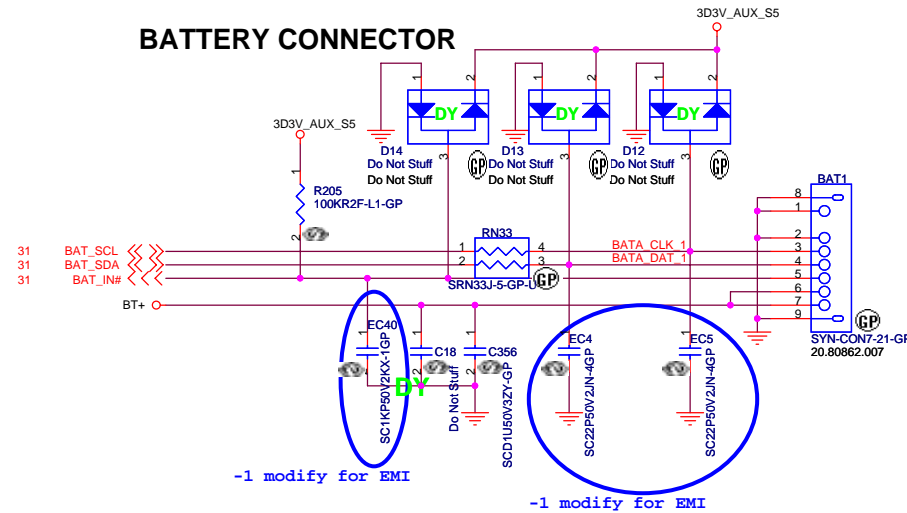
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1D25V/1D5V/0D9V		
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

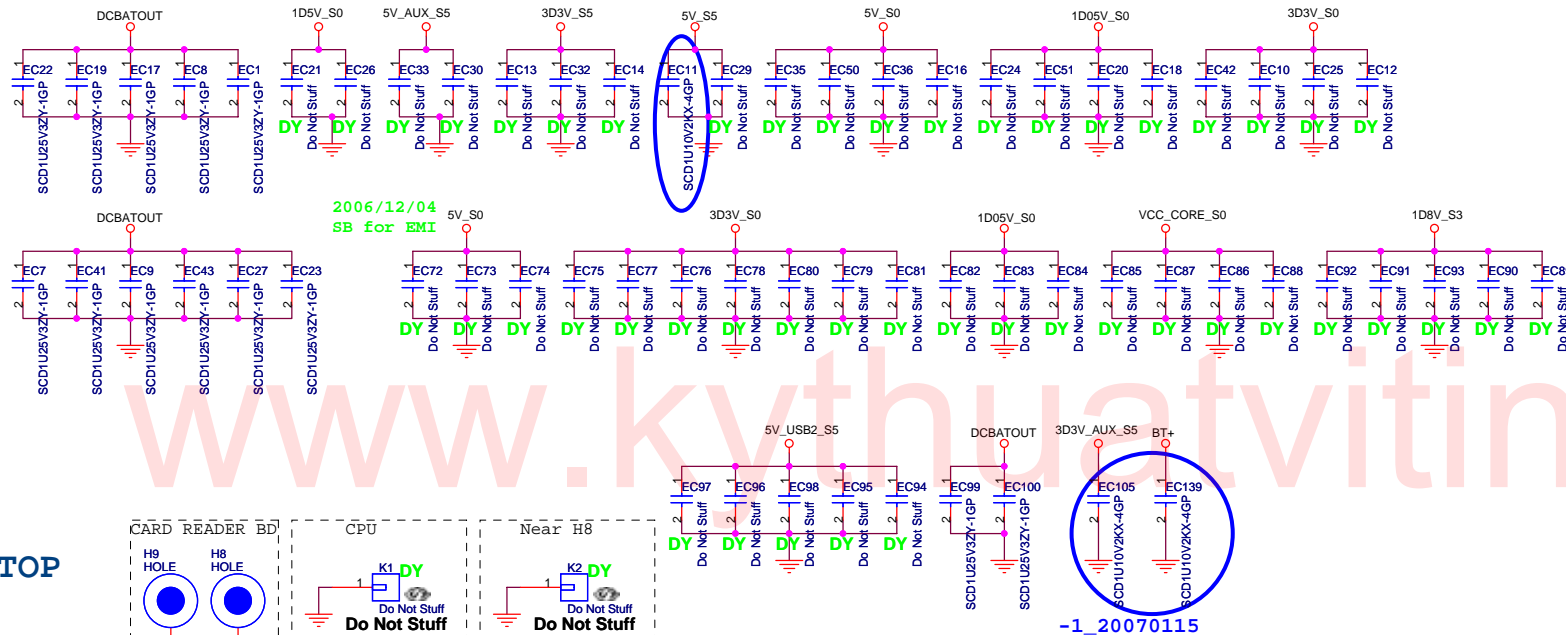


55.4H001.S03G

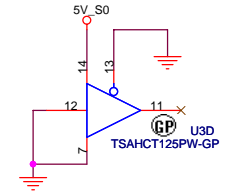
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Title		
AD/BATT CONN		
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EMI Capacitor



Unused gate



KBC JTAG Test Pad

31,32	KCOL1	<<<	KCOL1		TP88	Do Not Stuff
31,32	KCOL2	<<<	KCOL2		TP91	Do Not Stuff
31,32	KCOL3	<<<	KCOL3		TP92	Do Not Stuff
31,32	KCOL4	<<<	KCOL4		TP90	Do Not Stuff
31,32	KCOL6	<<<	KCOL6		TP89	Do Not Stuff
31,32	KCOL7	<<<	KCOL7		TP93	Do Not Stuff

DFX Test Point

3D3V_AUX_S5				TP97	Do Not Stuff
3D3V_S5				TP102	Do Not Stuff
5V_S5				TP100	Do Not Stuff
4,16,34 H_PWRGD				TP31	Do Not Stuff
28,31,34 S5_ENABLE				TP86	Do Not Stuff
4,6 H_CPUIRST#				TP39	Do Not Stuff

Test Point放在Dimm Door打開可量測處

55.4H001,S03G

緯創資通 **Wistron Corporation**
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Title			
EMI/Spring/Boss			
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	Biwa		-1
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